

USER MANUAL

**HSM/UM9808
SPHERIC Demo Board
Version 1.0**



REVISION HISTORY

Version	Remarks
1.0	First release



Purchase of Philips I²C components conveys a license under the Philips I²C patent to use the components in the I²C system, provided the system conforms to the I²C specifications defined by Philips.

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Version 1.0**

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IOM-2

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Preface

This User Manual describes a small demo board for speech recognition applications. The PCB contains a digital signal processor (DSP) called SPHERIC (Speech Recognizer IC, SBF1001HL), flash memory, SRAM and an I²C-bus I/O-expander and can be used in microcontroller systems or in conjunction with a personal computer (e.g. for demonstration purposes).

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1. General Description

The SPHERIC Demo Board consists of the basic elements for a speech recognition application as well as some optional features by keeping the size of the PCB moderate. The main components are the SPHERIC itself, flash memory, static RAM (optional), an address decoder (optional), a clock generator and divider and an I²C-bus I/O-expander. More application specific parts are the power supply, the reset generation and the input and output connectors, which also occupy large areas on the PCB. For that reason two additional subboard connectors were introduced to allow interfacing to other application specific (customer specific) hardware. When using the sub-board connector it is possible to cut the connector and/or the power supply area from the main part of the PCB.

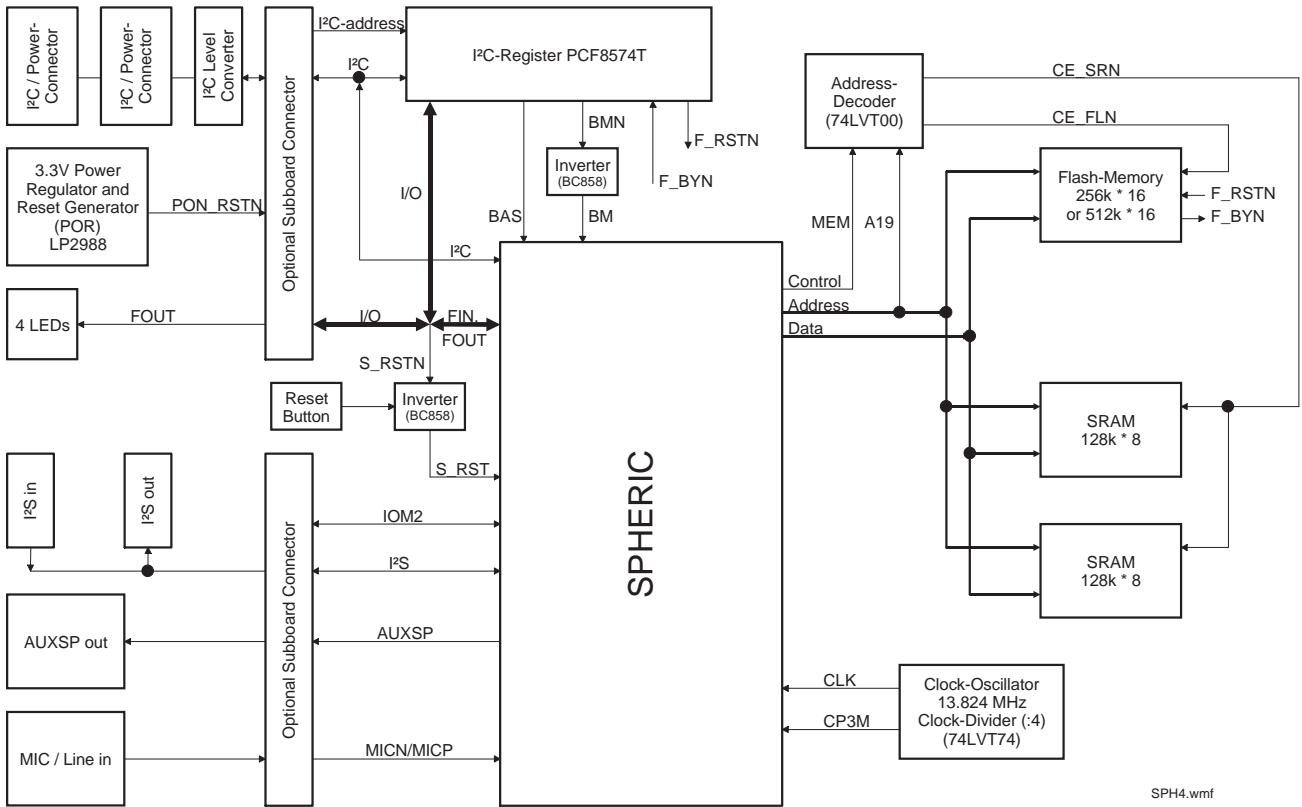


Fig.1 Blockdiagram of the SPHERIC Demo Board

2. Functional Description

2.1 Analog Audio Input

The MICN/MICP lines of the SPHERIC are used to interface a line input or a symmetrical or asymmetrical microphone with optional bias power supply. The diagrams below show the pins of the optional subboard connector and one jumper used for audio input connectivity. A few jumpers on CON1 are required to set up the board for either line input or microphone input. The jumper J1 (Mic) is set, if a microphone is used. The jumper setting needs not to be modified unless the signal source is to be replaced.

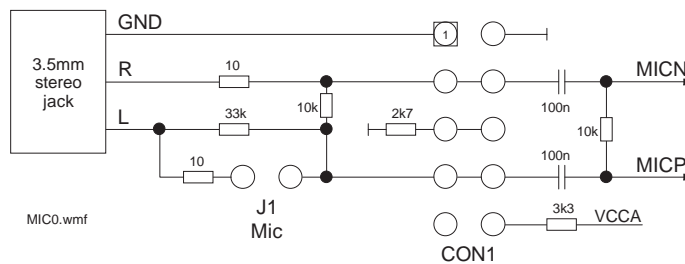


Fig.2 Board configuration of the audio input connector

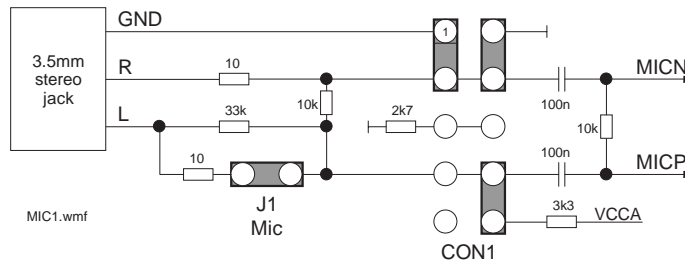


Fig.3 Jumper configuration for asymmetrical microphone with bias supply

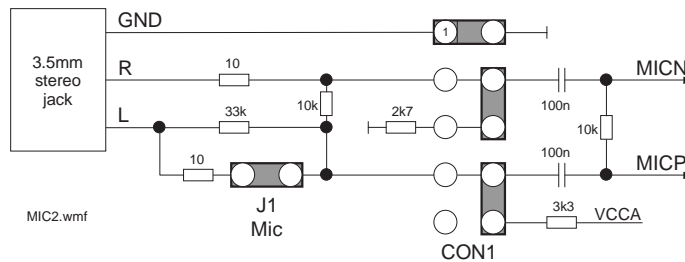


Fig.4 Jumper configuration for symmetrical microphone with shielded cable and bias supply

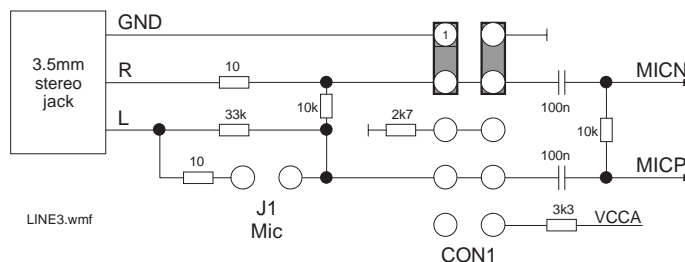


Fig.5 Jumper configuration for line input (for use with mono plug)

2.2 Analog Audio Output

The AUXSP line out of the SPHERIC is used to either interface an active PC sound system or a high impedance headphone. The diagram below shows the corresponding pins of the optional subboard connector. The jumpers have to be set once for the output device.

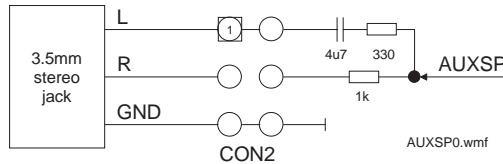


Fig.6 Board configuration of the audio output connector

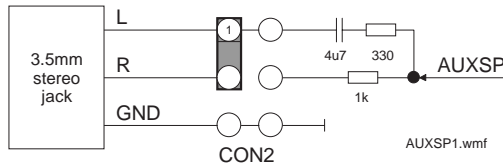


Fig.7 Jumper configuration for output on both stereo channels (AC coupling)

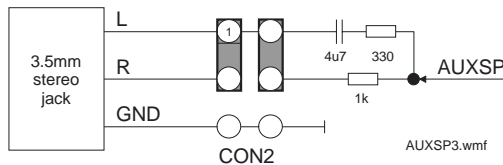


Fig.8 Jumper configuration for output on both stereo channels (DC coupling)

2.3 I²S-Interface

There are two optional connectors foreseen on the SPHERIC Demo Board to interface I²S signals. The input can be configured to SD0 or SD1 pin of the SPHERIC (jumper on CON6 at pins 3 and 4 or pins 1 and 2), the output is fed directly to the connector. The SPHERIC operates as I²S slave device and gets the serial clock (SCK) and word select (SWS) from an external master. The I²S interface can be used alternatively to the analog audio codec or the digital IOM2 interface. The mode is selected by the software running on the SPHERIC.

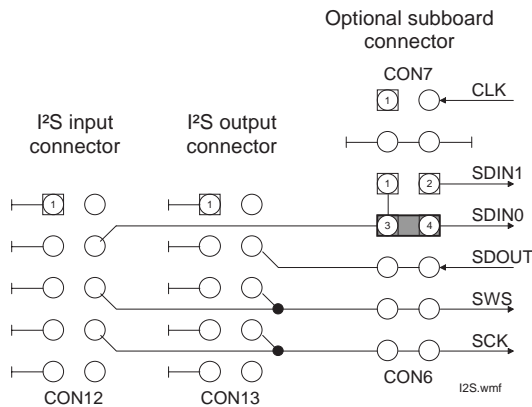


Fig.9 Diagram of the I²S connectors

2.4 IOM-2 Interface

The IOM-2 lines of the SPHERIC are fed to four pins of the optional subboard connector. The lines IOM2_DD and IOM2_DU have an 1k pull-up resistor each. The IOM2 interface can be used alternatively to the analog audio codec or the digital I²S interface. The mode is selected by the software running on the SPHERIC.

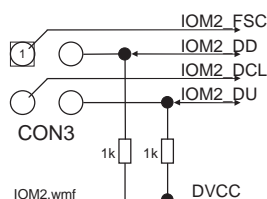


Fig.10 Pin assignment of the IOM2 interface connector CON3

2.5 Power Supply and Reset Generation

The SPHERIC Demo Board is a pure 3.3V design. To ease interfacing, a voltage regulator with built-in power on / power failure reset generation is used. The regulator allows interfacing to a 5V power supply. Even if the regulator is not used (bypassed with jumper J2, pin 1 to pin 2) the circuit is used to monitor the incoming 3.3V and to generate the reset signal. If the input voltage is too low, the reset signal out of the regulator remains active. After approx. 70 ... 100 ms after power-up the reset is deasserted. The reset out of the regulator is fed via a jumper on the subboard connector CON5 (pin 23 to pin 21). The reset button is connected directly to the inverting transistor (see Fig.11 on page 11).

The power consumption of the SPHERIC demo board depends on the application running on the SPHERIC. The input current has been measured to approx. 45 mA (after reset) to 90 mA (during flash erase operation).

2.6 Clock Generation

A (pre-) programmable 3.3V crystal oscillator is used to generate the 13.824 MHz clock for the SPHERIC. This clock is also available on the subboard connector. The clock for the SPHERIC audio codec is derived with a divider (div. by 4 using the two flip-flops out of the 74LVT74).

2.7 Memories and Address Decoding

Two types of flash memories are foreseen on the SPHERIC Demo Board. Either 256k16 or 512k16 flashes can be used (e.g. AM29LV400 or AM29LV800). Two resistors (R19 and R20) need to be assembled according to the flash type: R19 = 0R and R20 = OPEN for AM29LV800; R19 = OPEN and R20 = 0R for AM29LV400. For the SRAM a TSOP32F package is used. At least three memory types seem to be suitable with a memory size of either 128k8 or 64k8: KM68V1000BLTI-7L (Samsung; 128k8); TC55V1001STI (Toshiba; 128k8); KM68V512 (Samsung; 64k8). SRAM need only to be assembled, if it is required by the software running on the SPHERIC. Since using a simple address decoding logic the memories can be accessed at baseaddresses of multiples of the memory size. The flash memory is located starting at address 0x00000, the SRAM starts at 0x80000.

2.8 I²C-Bus-Interface

The I²C-bus interface of the SPHERIC Demo Board is equipped with level shifters (two fieldeffect transistors) to allow directly the operation with 5V level I²C-bus applications. It is also possible to operate the SPHERIC Demo PCB with 3.3V external I²C-bus levels without modifications.

Via the I²C-bus it is possible to access an I/O-expander (see below) and the SPHERIC. After power-up the SPHERIC has a default hard-wired device address (1Ah [7bit notation]; 34h [8bit notation]; '0011010' bin, to be followed by R/W control bit). This address can be modified in two ways: when boot mode (BM) = 1, the device address is read out of the Y-MEM at address 0x00001, furthermore the software running on the SPHERIC is able to modify the register containing the device address. For details see SPHERIC datasheet.

2.9 I²C-Bus I/O-Expander

An 8 bit I²C-bus I/O-expander is used for extended interfacing to the SPHERIC and the flash memory features. It is possible to reset the flash memory as well as the SPHERIC and to set the SPHERIC boot mode. The default after power-on is to boot from flash memory; BAS = 1; BM = 0). Some I/O-lines are free for future use (ports 7, 3, 2 and 1) and can be assigned to SPHERIC I/O lines via jumper settings (see below). The I²C-slaveaddress of the device can be set via jumpers (address bits A2 and A1) and resistors (R6 and R14 for bit A0). This allows the operation of multiple SPHERIC Demo Boards on one I²C-bus. The following tables show the jumper and resistor settings, the corresponding slaveaddress and the assignment of the I/O-lines.

TABLE 1 Jumper settings for the I²C slaveaddress of the PCF8574T

A2 CON5 pin 25 to CON4 pin 1 (DGND)	A1 CON5 pin 26 to CON4 pin 2 (DGND)	A0		Slaveaddress	
		R6 (pull-up)	R14 (pull-down)	7bit notation	8bit notation
closed (low)	closed (low)	open	0R	20h	40h
closed (low)	closed (low)	10k	open	21h	42h
closed (low)	open (high)	open	0R	22h	44h
closed (low)	open (high)	10k	open	23h	46h
open (high)	closed (low)	open	0R	24h	48h
open (high)	closed (low)	10k	open	25h	4Ah
open (high)	open (high)	open	0R	26h	4Ch
open (high)	open (high)	10k	open	27h	4Eh

TABLE 2 I/O-line assignment of the PCF8574T

Bit / Port	7	6	5	4	3	2	1	0
Value	80h	40h	20h	10h	08h	04h	02h	01h
Signal Name [option]	n.c. [F_BYN]	F_RSTN	BAS	BMN	n.c. [FOUT0]	n.c. [FIN2]	n.c. [FIN1]	S_RSTN

After power-up the default for the PCF8574T I/O-lines is high (FFh; high via internal pull-up; see note below concerning SPHERIC input cell pull-down resistors). This results in external (flash) memory boot-mode (BM=0) and cold start (BAS=1: bootstrap procedure is started at ZMEM address 0xF00).

To invoke a reset of the SPHERIC (cold or warm start, ext. memory boot or I²C boot), the PCF8574T should be read and rewritten with the desired settings for the bits BMN and BAS (the other bits should get the previous read value). Furthermore the databyte should be send three times so that for the S_RSTN line a low active reset pattern is generated. This can be done in one I²C transmission.

Read from PCF8574T via I²C bus:

S 27h **R** databyte (e.g. FFh) **P**

[**S**: start condition; **R**: read operation]

[**P**: stop condition; **W**: write operation]

Write reset pattern to PCF8574T via I²C bus:

S 27h **W** FFh FEh FFh **P** BAS=1; BMN=1 (BM=0): cold start; boot from external (flash) memory
S 27h **W** EFh EEh EFh **P** BAS=1; BMN=0 (BM=1): cold start; waiting for I²C download of the boot program
S 27h **W** DFh DEh DFh **P** BAS=0; BMN=1 (BM=0): warm start (restart current program at ZMEM 0x000)
S 27h **W** CFh CEh CFh **P** BAS=0; BMN=0 (BM=1): warm start (restart current program at ZMEM 0x000)

2.10 SPHERIC User I/O - Lines

The SPHERIC user I/O-lines are fed to the optional subboard connector. The outputs are also fed to four LEDs which are located in the connector area. A high signal on the pins will activate the appropriate LED. FOUT3 can be used to reset the flash memories if a jumper is set on CON5. This offers the opportunity to invoke a flash reset via software running on the SPHERIC. FOUT0, FIN1 and FIN2 can be fed to port 3, port 1 and port 2 of the PCF8574 via jumper on the subboard connector CON5. Optionally the status of the flash memory (F_BYN at FIN0) can be read back via port 7 of the PCF8574 when an appropriate jumper is set.

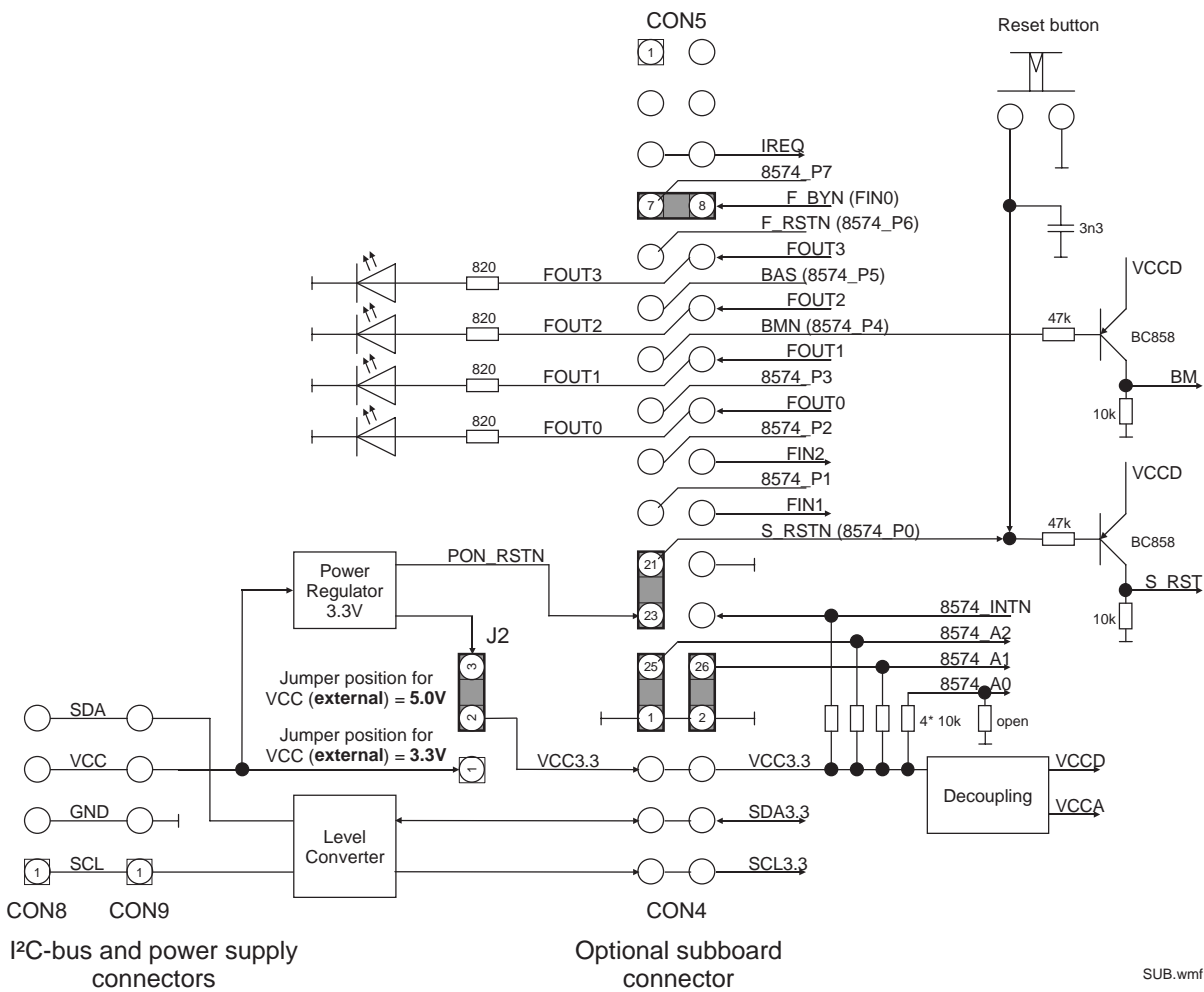


Fig.11 Optional subboard connector for power supply, I²C-bus and control I/O

Note 1:

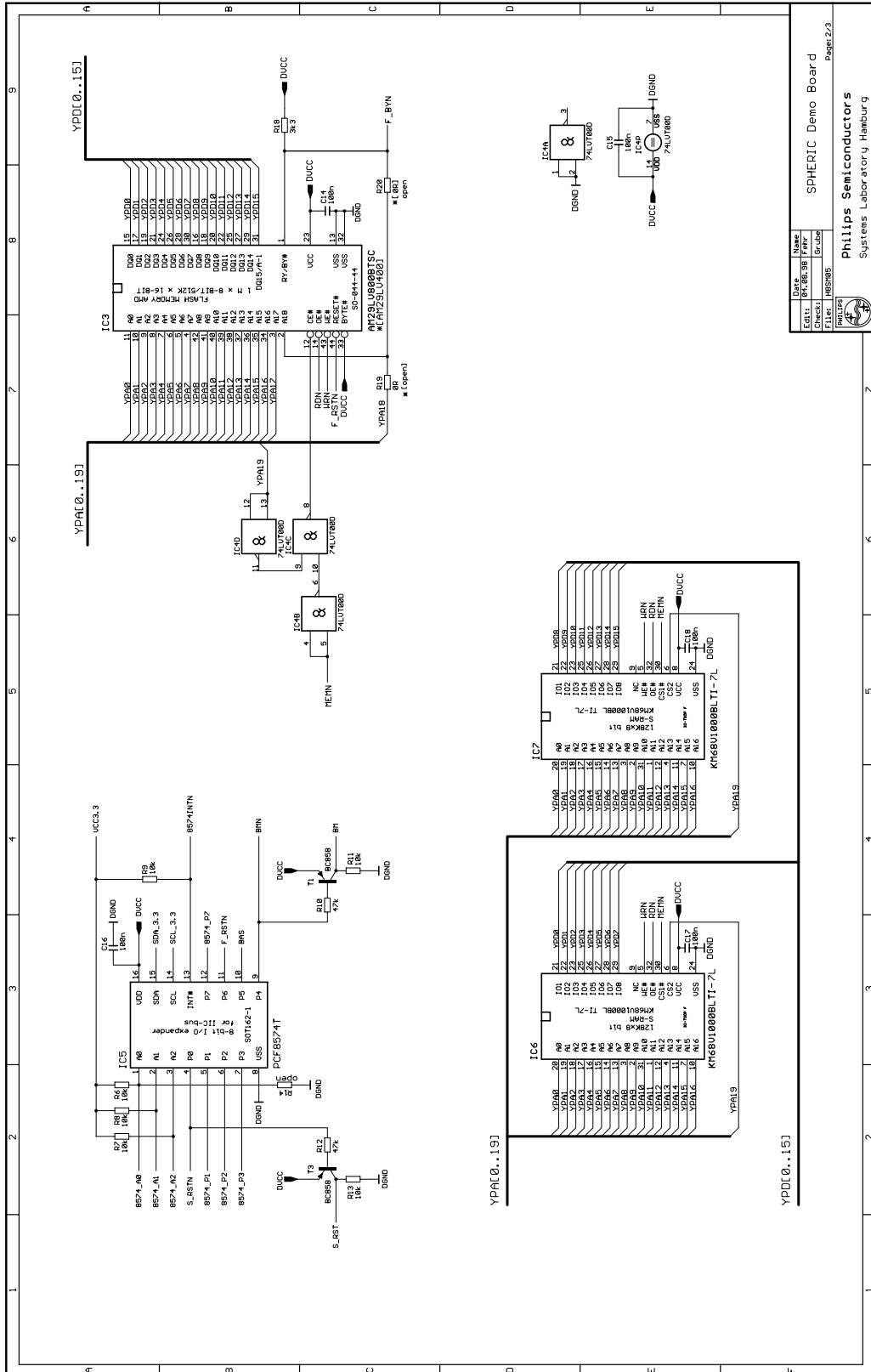
To adapt different LEDs to the board the resistors R32 ... R35 can be reduced down to 470 ohms. A further reduction leads to a current of more than 3 mA (max. current for SPHERIC FOUT cell). Red low current LEDs are preferred due to their higher efficiency.

Note 2:

Since SPHERIC has pull-down resistors at most of its input cells it is required to add pull-up resistors when using high ohmic sources (for logical high level) like the PCF8574T. For the signal BAS (PCF8574T bit 5) an additional 4k3 resistor is mounted on the PCB to ensure stable reset and boot behaviour.

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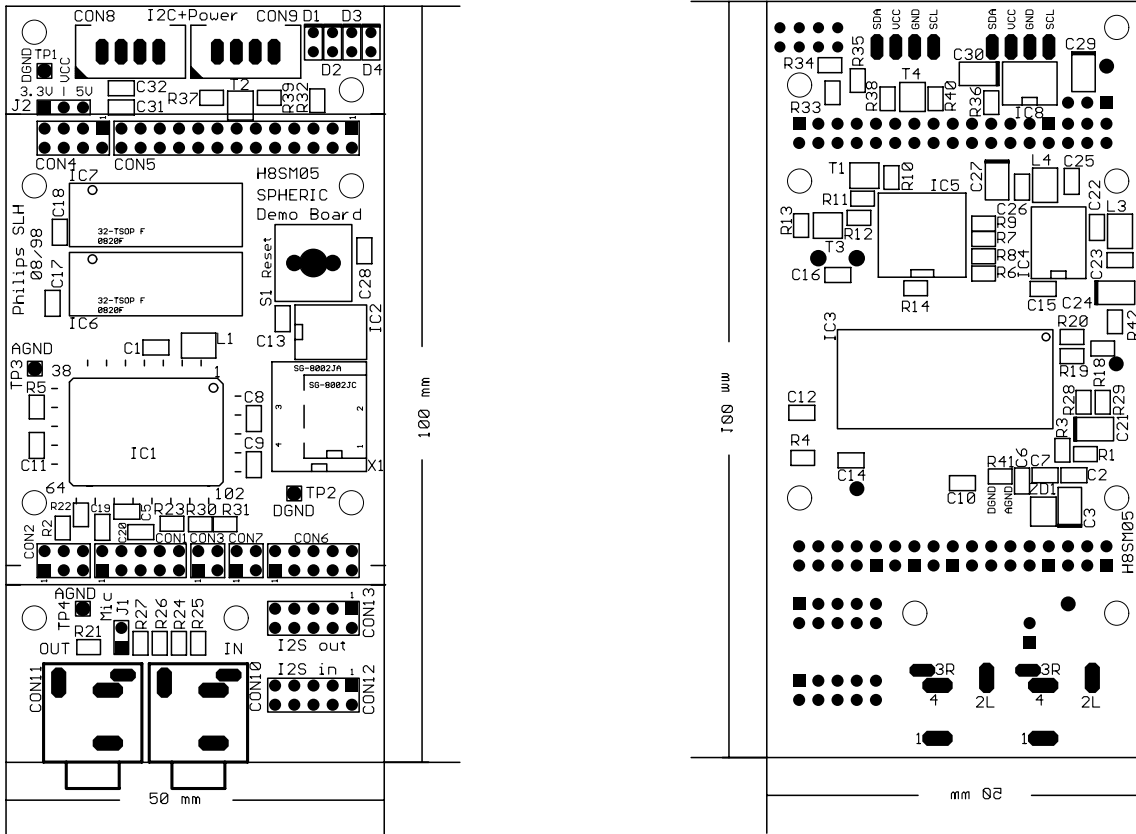
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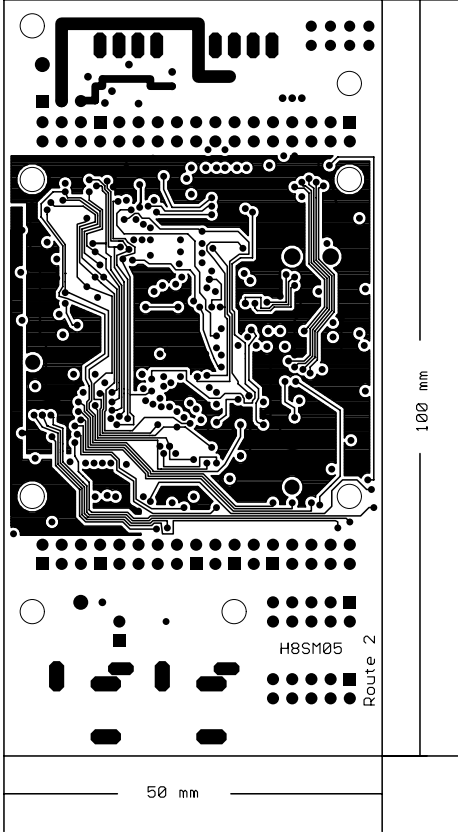
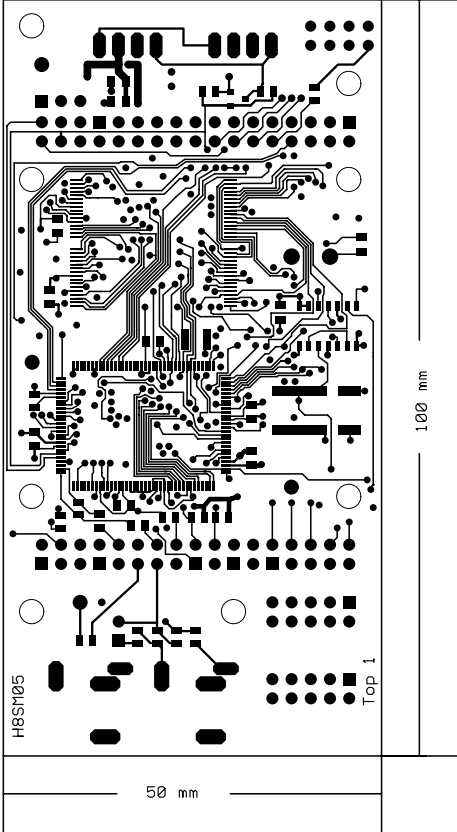
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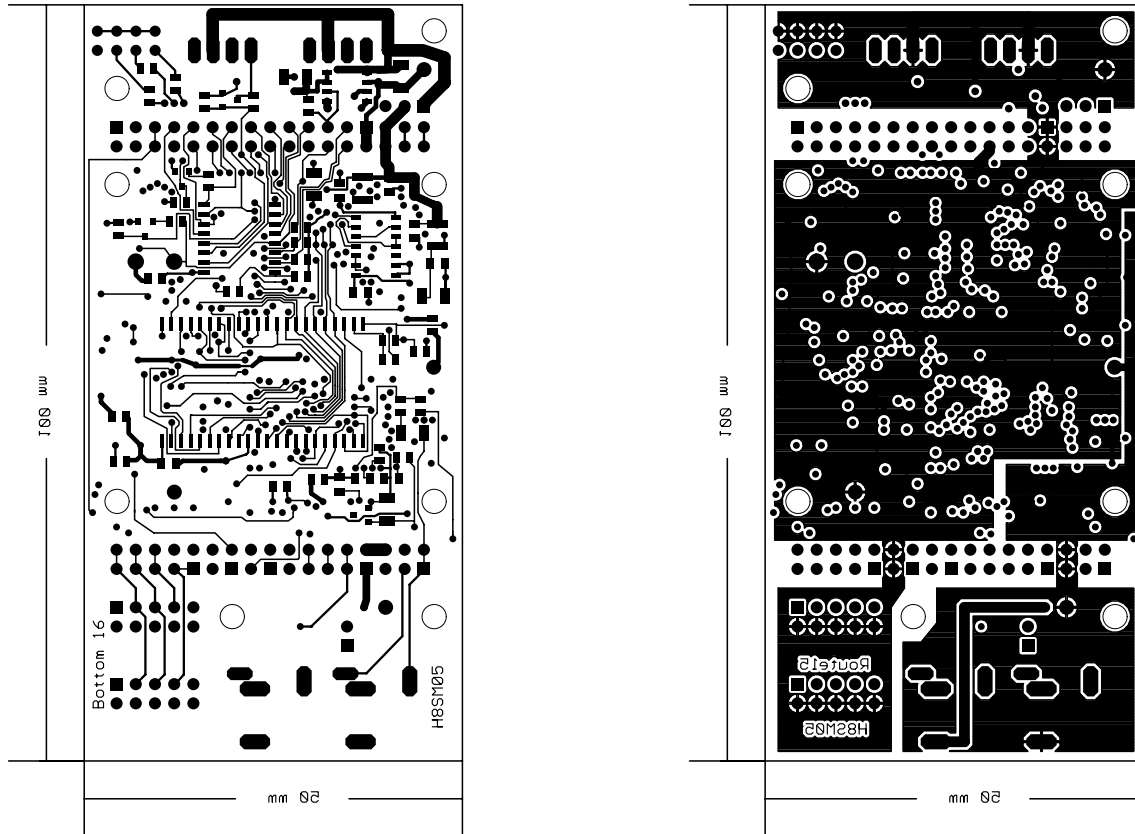
3.2 Layout of H8SM05



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3.3 References

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